OAKLAND UNIVERSITY

Department of Electrical & Computer Engineering (ECE)
Microelectronics & Bio-Inspired Systems Design Lab (MSDL)

ECE4132/ECE5132, CRN: 11350/11351

VLSI CIRCUITS DESIGN OF DIGITAL CHIPS

W2018: January 3rd –to- April 25th, 2018 (Spring Break Feb. 19th –to- 23rd, 2018)
January 4th, 2018, Edited March 1st, 2018

Instructor: Professor Hoda S. Abdel-Aty-Zohdy, Ph.D., Director of the Microelectronics & Bio-Inspired Systems Design Lab (MSDL)
Office Telephone: 248-370-2243 ***Office Number:*** EC 426
email: ***zohdyhsa@oakland.edu***
Class Schedule: T & R 5:30 –to- 7:17pm ***Classroom:*** SFH 363
Office Hours: W 4:00 –to- 5:00pm, R 7:30pm –to- 8:30pm, or by appointment.
Laboratory: **Mentor Graphics™ industry standard VLSIC Design Automation CAD tools Suit.**
Instructed Lab Session: **T 7:30 –to-10:30pm, EC 455, and the MSDL lab, EC 366**
TA (LAB Instructor):Mr. Klajdi Lumani
Prerequisite: Interest in Integrated Circuits (VLSICs) Design and Applications; Background in Electronic Circuits and/or Solid-state devices.
Credit Hours: 4
Text and References:

(1) **"**CMOS VLSI Design: A Circuits and Systems Perspective," by N. Weste and D. M. Harris, Addison Wesley, 4th Edition, ISBN 10: 0-321-54774-8; ISBN 13: 978-321-54774-3, 2011.
http://pages.hmc.edu/harris/cmosvlsi/4e/index.html

(2) "CMOS Digital Integrated Circuits: A First Course", by C. Hawkins, J. Segura, and Payman Zarkesh-Ha, SciTech, ISBN 978-1-61353-002-3, 2013.

(3) "Chip Design for Submicron VLSI: CMOS Layout and Simulation," by John Uyemura, ISBN# 0-534-46629-X, Thompson, 2006.

(4) "Introduction to VLSI Circuits and Systems." John P. Uyemura, ISBN#0-471-12704-3, John Wiley & Sons, Inc., 2002

The following books for optimization of Digital Designs:

(5) "Synthesis and Optimization of Digital Circuits," by De Micheli.

(6) "Algorithms for VLSI Physical Design Automation," by Sherwani.

(7) "Digital Integrated Circuits: a Design Perspective (2nd edition)," by Rabaey, Chandrakasan, Nikolic.

Final Exam: April 19th, 2018, 7:00 –to- 10:00pm ➔ PROJECTS PRESENTATIONS

Catalog Description:
CMOS Very Large Scale Integrated Circuits (VLSIC) design methodology for chip implementation and evaluation. Functional, digital, circuit, device, and layout levels of abstraction. CMOS IC Design of combinational and sequential digital systems. Switching characteristics of MOS Inverters, logic, and transmission gates. Static, clocked, and

dynamic logic gates Application Specific ICs design and prototype chip projects using industrial standard CAD tools suite. With Laboratory.

Course Objectives:
The course offers a modern and timely view of Very Large Scale Integrated Circuits (VLSICs) using Complementary Metal Oxide Semiconductor (CMOS) building blocks for digital ICs. Focus on CMOS inverters and Transmission gates with power and timing performance. Regardless of one's integrated circuit (IC) design back ground, this course provides the **theory behind, and the hands-on design and implementation of, CMOS VLSICs design methodology for chip prototype with processing, and evaluation.**
The course is project oriented.
Projects involve designs of data converters, signal control and processing, and much more. **Students design Application Specific Integrated Circuits (ASICs) for practical applications using the industrial standard CAD tools Mentor Graphics™ Suite** at TSMI, or On-Semiconductor 0.5um, or the IBM 0.18u.m technology.

Course Material, on MOODLE:
All reading assignments, solved problems, homework assignments, and solutions.
Laboratory tutorial assignments and other relevant information will be posted on Moodle.

Grading System

Midterm Exams (Two)	30%
Laboratory Tutorials/assignments	15%
Homework Assignments	15%
Project:	**40%**
Project Proposal:	5%
Progress Report:	5%
Project Presentation:	5%
Project Design and Report:	20%
Chip Test Chapter	5%

COURSE CONTENTS:

1. Introduction to Micro and Sub-micro (~Nano) Technology for VLSICs and Digital Systems (Lecture Notes and Lect-0 power point, posted material)
2. Design Methodology and Hierarchy (Wolfe power-point & Chapter 14)
3. **Mentor Graphics™ = *MG™* CAD tools Laboratory Tutorials 1 & 2**
4. Introduction to CMOS VLSIC Design. (Chapter 1 Weste)
5. Solid-State Devices Basic Equations (Handout)
6. MOS Device, Threshold Voltage, I-V characteristics (Lecture notes+ Reinhard-Chap3)
7. The MOS Transistor Theory (Chapter 2 Weste)
   - C-V characteristics
   - Non-Ideal I-V Characteristics
   - DC Transfer Characteristics
8. CMOS Fabrication (Processing Technology). (Chapter 3 Weste)

9. **MOS Circuit Simulation (SPICE), Lab # 3 (**Chapter 8)
10. Integrated Circuit Resistors and Capacitors: Delay, Power, and interconnects
    a. Delay (Chapter 4, …)
    b. Power (Chapter 5)
    c. Interconnect and Robustness (Chapters 6 & 7 Weste,)

10. CMOS VLSIC Design Projects Start February.
11. CMOS Combinational IC Design (Chapter 9)
12. Sequential IC Design. (Chapter 10)
13. ***MG*™ CAD tools Laboratory Tutorials 4, 5**
14. Addition/Subtraction; Comparators; Counters (Chapter 11)
15. Static Logic Gates & Clocked Gates. (Chapter 12)
16. Array & Special Purpose subsystems (time permitting) (Chapters 12 and 13)

ABET/Course Objectives:

The course is the first in VLSIC, and thus applications are limited to Digital designed and Fabricated IC Chips.

(1) To solve challenges in Integrated Circuits Design and layout techniques.

(2) To determine CMOS switching characteristics (Rise-time, Fall-time, and propagation delays).

(3)To design, simulate, and prepare for fabrication a Digital CMOS Integrated Circuit projects.

(4)To demonstrate effective technical communications through projects presentations and written technical reports.

(5) To use Industrial Standards CAD tools for VLSIC Chips, (Mentor Graphics™).

ECE485/585 Laboratory Assignments:

1. MG Lab #1: Mentor Graphics™ Getting Started, UNIX, MG™ Feb 6th, 2018
2. MG Lab #2: Mentor Graphics™ Working with **Verilog, and QuestaSim** Feb. 13th, 2018
3. MG Lab #3: Mentor Graphics™ Full Custom Design using MG's **PYXIS™** Feb 26th- March 5th, 2018
4. MG Lab # 4 Mentor Graphics™ LOGIC SYNTHESIS using **Leonardo Spectrum™** March 12th, 2018
5. MG Lab # 5 Mentor Graphics™ Schematic Entry USING **Pyxis Schematic,** March 19th, 2018
6. MG Lab # 6 Mentor Graphics™ Verilog Netlist to Schematic, to Layout, Mach 26th, 2018
7. MG Lab **#** 7 Mentor Graphics™ Layout Verification USING **Calibre™**
8. MG Lab # 8 Mentor Graphics**™ Stuffed Pad Frames**
9. MG Lab # 9 Mentor Graphics™- Post Layout SPICE Simulation Using **Calibre™ and ADIT™**

10. MG Lab # 10 Mentor Graphics ™ **SEMICUSTOM DESIGN SCHEMATIC DRIVEN LAYOUT**

11. Mentor Graphics ™ **GDS-II** files preparation and CHIP submission to **MOSIS**

After Tutorial (Lab) #4 you will be ready to start the design of your Project.
The following labs are to guide you in the process to go from a concept to a submitted IC CHIP

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EXAM#1 **March 8th, 2018**

EXAM#2 **April 10th, 2018, or April 12th, 2018**

Project Presentations and Reports Due on April 19th, 2018